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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/604,744

08/14/2003

SUNG-MAO WU

9720-US-PA

1743

31561

7590

10/03/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

PATEL, ISHWARBHAI B

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/604,744

Applicant(s)

WU, SUNG-MAO

Examiner

Ishwar (I. B.) Patel

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al, US Patent No. 6,734,370, (Yamaguchi), and further in view of Handforth et al., US Patent No. 6,876,085 (Handforth).

Regarding claim 1, Yamaguchi, in figure 1B, discloses a printed circuit board, at least comprising: a plurality of patterned circuit layers (electrically conductive traces on substrate 22); an insulation layer (substrate 22) between the patterned circuit layers for isolating the patterned circuit layers from each other, wherein the insulation layer and the patterned circuit layers together form a laminated layer (laminated board, see figure 1B); and at least one side circuit (electrically conductive line 32 along side 30) on a sidewall of the laminated layer for electrically interconnecting at least any two of the patterned circuit layers (column 5, line 38-42).

Yamaguchi does not explicitly disclose the at least one side circuit has a shape structure so that impedances of the sidewall circuits and the patterned circuit layers are matched with each other.

Handforth, on column 1, line 25-35, recites that mismatching of the impedance and problems associated with that in connecting conductive traces are known and has to be solved to reduce the cross talk to adjacent signals and to have efficient performance of the device. Handforth et al., further recites to form signal traces in various width to optimize impedance matching, (page 3, line 38-39). Also, Handforth, (in figure 5, on page 4, line 23-37), recites the traces with tapered shape (varying width) and states that a skilled artisan will understand that many possible dimensions will provide advantageous.

Further, this is a structural claim. Yamaguchi, discloses all the features of the structure as claimed. Therefore, a person of ordinary skill in the art would consider the patterned circuit layers, including the side traces layers, of Yamaguchi to have matched impedance for the efficient performance of the device.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to have the circuit board of Yamaguchi with the at least one side circuit has a shape structure so that impedances of the sidewall circuits and the patterned circuit layers are matched with each other, as taught by Handforth, in order to reduce cross talk and to have efficient performance of the device.

Regarding claim 3, the modified circuit board of Yamaguchi further discloses the at least one side circuit includes a uniform width (uniform width of element 32, see figure 1B).

Regarding claim 4, the modified circuit board of Yamaguchi further discloses all the features of the claimed invention as applied to claim 1 above, but does not disclose the at least one side circuit includes a varying width.

Handforth, as applied to claim 2 above, recites signal traces in various width to optimize impedance matching, (page 3, line 38-39), and traces with tapered shape (figure 5, on page 4, line 23-37).

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to vary width of the sidewall circuits to match the impedance of the patterned circuits to optimize impedance matching to have reduced cross talk and efficient performance of the device.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Yamaguchi, with the at least one side circuit having a varying width, as taught by Handforth, in order to match the impedance of the patterned circuits to optimize impedance matching to have reduce cross talk and efficient performance of the device.

Regarding claim 5, the modified circuit board of Yamaguchi further discloses all the features of the claimed invention as applied to claim 1 above the but does not disclose at least one side circuit includes a trapezoidal shape.

Handforth, as applied to claim 2 above, recites signal traces in various width to optimize impedance matching, (page 3, line 38-39), and traces with tapered shape (figure 5, on page 4, line 23-37).

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide sidewall circuits with a trapezoidal shape (tapered shape) to match the impedance of the patterned circuits to optimize impedance matching to have reduced cross talk and efficient performance of the device.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Yamaguchi, with the at least one side circuit having a trapezoidal shape, as taught by Handforth, in order to match the impedance of the patterned circuits to optimize impedance matching to have reduce cross talk an efficient performance of the device.

Response to Arguments

3. Applicant's arguments filed July 22, 2005 have been fully considered but they are not persuasive.

Applicant argues that in Yamaguchi, the side circuit is just for interconnection between the patterned circuit layers but is not designed with impedance matching and states that the secondary art of Handforth does not disclose impedance matching circuit is formed on the sidewall of the circuit but discloses impedance circuit design for overlapping and direct contact, the design of Yamaguchi is conflict with the side circuit of the side wall and Handforth doe not provide sufficient motivation to modify Yamaguchi into the present invention.

These are not found persuasive. The primary reference of Yamaguchi discloses the interconnection of patterned circuit by the side circuit and if the interconnection is

there, it better be matched otherwise too much noise and scattering. Also, the secondary art of Handforth is used for the teaching of the impedance matching by varying the shape of the trace. The examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. *In re Nomiya*, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what a combination of disclosures taken, as a whole would suggest to one of ordinary skill in the art. Further, one cannot show non-obviousness by attacking references individually where, as here the rejections are based on combination of references.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Amparan et al., US Patent No. 6,737,931 in figure 1A-1B, discloses transmission line portion (14) with varying width (w) dimension for impedance matching, column 3, line 45-60.

Shingyoji et al., US Patent No. 6,331,806, in figure 1, discloses a connecting ribbon (11e) having various shapes (shown in figure 5A-5D) as a part of regulating impedance.

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5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

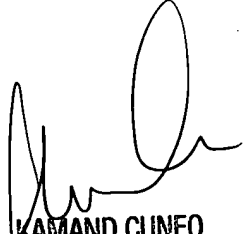
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
September 29, 2005



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SUPERVISORY PATENT EXAMINER
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